Course code	Course Name	L-T-P –Credits	Year of Introduction
CS405	COMPUTER SYSTEM ARCHITECTURE	3-0-0-3	2016

Course Objectives:

- To impart a basic understanding of the parallel architecture and its operations
- To introduce the key features of high performance computers

Syllabus:

Basic concepts of parallel computer models, SIMD computers, Multiprocessors and multi-computers, Cache Coherence Protocols, Multicomputers, Pipelining computers and Multithreading.

Expected outcome :

The Students will be able to :

i. summarize different parallel computer models
ii. analyze the advanced processor technologies
iii. interpret memory hierarchy
iv. compare different multiprocessor system interconnecting mechanisms
v. interpret the mechanisms for enforcing cache coherence
vi. analyze different message passing mechanisms
vii. analyze different pipe lining techniques
viii. appraise concepts of multithreaded and data flow architectures

Text Book:

- K. Hwang and Naresh Jotwani, Advanced Computer Architecture, Parallelism, Scalability, Programmability, TMH, 2010.

References:

1. H P Hayes, Computer Architecture and Organization, McGraw Hill, 1978.
2. K. Hwang & Briggs , Computer Architecture and Parallel Processing, McGraw Hill International, 1986
3. M J Flynn, Computer Architecture: Pipelined and Parallel Processor Design, Narosa Publishing House, 2012.
4. M Sasikumar, D Shikkare and P Raviprakash, Introduction to Parallel Processing, PHI, 2014.
5. P M Kogge, The Architecture of Pipelined Computer, McGraw Hill, 1981.
6. P V S Rao , Computer System Architecture, PHI, 2009.
7. Patterson D. A. and Hennessy J. L., Morgan Kaufmann , Computer Organization and Design: The Hardware/Software Interface, Morgan Kaufmann Pub, 4/e, 2010.

Course Plan			
Module	**Contents**	**Hours**	**End Sem. Exam Marks**
I	Parallel computer models – Evolution of Computer Architecture, System Attributes to performance, Amdahl's law for a fixed workload. Multiprocessors and Multicomputers, Multivector and SIMD computers, Architectural development tracks, Conditions of parallelism.	6	15%
II	Processors and memory hierarchy – Advanced processor technology- Design Space of processors, Instruction Set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar and vector processors, Memory hierarchy technology.	8	15%
FIRST INTERNAL EXAM			
III	Multiprocessors system interconnects - Hierarchical bus systems, Cross bar switch and multiport memory, Multistage and combining networks. Cache Coherence and Synchronization Mechanisms, Cache Coherence Problem, Snoopy Bus Protocol, Directory Based Protocol, Hardware Synchronization Problem	7	15%
IV	Message Passing Mechanisms-Message Routing schemes, Flow control Strategies, Multicast Routing Algorithms. Pipelining and Superscalar techniques – Linear Pipeline processors and Nonlinear pipeline processors	8	15%
SECOND INTERNAL EXAM			
V	Instruction pipeline design, Arithmetic pipeline deign - Super Scalar Pipeline Design	8	20%
VI	Multithreaded and data flow architectures - Latency hiding techniques, Principles of multithreading - Multithreading Issues and Solutions, Multiple context Processors, Fine-grain Multicomputer- Fine-grain Parallelism. Dataflow and hybrid architecture	8	20%
END SEMESTER EXAM			

Question Paper Pattern (End semester exam)

1. There will be ***FOUR*** parts in the question paper – **A, B, C, D**
2. **Part A**
   a. **Total marks : 40**
   b. *TEN* questions, each have **4 marks**, covering **all the SIX modules** (*THREE* questions from **modules I & II**; *THREE* questions from **modules III & IV**; *FOUR* questions from **modules V & VI**).
   All the TEN questions have to be answered.
3. **Part B**
   a. **Total marks : 18**
   b. *THREE* questions, each having **9 marks**. One question is from **module I**; one question is from **module II**; one question ***uniformly*** covers **modules I & II**.
   c. ***Any TWO*** questions have to be answered.
   d. Each question can have ***maximum THREE*** subparts.
4. **Part C**
   a. **Total marks : 18**
   b. *THREE* questions, each having **9 marks**. One question is from **module III**; one question is from **module IV**; one question ***uniformly*** covers **modules III & IV**.
   c. ***Any TWO*** questions have to be answered.
   d. Each question can have ***maximum THREE*** subparts.
5. **Part D**
   a. **Total marks : 24**
   b. *THREE* questions, each having **12 marks**. One question is from **module V**; one question is from **module VI**; one question ***uniformly*** covers **modules V & VI**.
   c. ***Any TWO*** questions have to be answered.
   d. Each question can have ***maximum THREE*** subparts.
6. There will be ***AT LEAST*** **60%** analytical/numerical questions in all possible combinations of question choices.